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Charge movement in a GaN-based hetero-structure field effect transistor structure with carbon doped buffer under applied substrate bias

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Charge trapping and transport in the carbon doped GaN buffer of a GaN-based hetero-structure field effect transistor (HFET) has been investigated under both positive and negative substrate bias. Clear evidence of redistribution of charges in the carbon doped region by thermally generated holes is seen, with electron injection and capture observed during positive bias. Excellent agreement is found with simulations. It is shown that these effects are intrinsic to the carbon doped GaN and need to be controlled to provide reliable and efficient GaN-based power HFETs.
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I. INTRODUCTION

GaN-based hetero-structure field effect transistors (HFETs) have matured during recent years. Devices delivering performance superior to those based on GaAs or Si technology are commercially available for RF applications.[1] Also devices for power applications have been introduced to the market recently.[2] The underlying physics for those devices are generally understood, but some effects like the current collapse (CC) phenomena and buffer breakdown have not been explained fully and can cause major restrictions to device performance. CC partly originates from surface effects, which can be suppressed by advanced device design, in particular, by the use of field plates, but is also related to charge trapping in the buffer,[3,4] in particular, under high voltage conditions.

The fact that both CC and electrical breakdown are related to the layers below the two dimensional electron gas (2DEG) shows that characterization of those layers is critical to delivering efficient, reliable power devices. Recent studies on vertical leakage currents in GaN power devices refer to current flow through the entire structure.[5,6] At low vertical electrical fields, though currents do not flow through the entire structure but can flow locally. To investigate charge transport in this regime, the ramped back biasing technique can be used.[7–9] Carbon containing buffer layers are not only known to prevent punch-through effects and improve vertical breakdown,[10,11] but are also linked to CC behavior.[12]

In this work, a structure containing a thick carbon doped GaN layer has been investigated by the back biasing technique. With the help of simulations, position and movement of charges could be identified and clearly linked to CC.

II. EXPERIMENTAL DETAILS

A GaN on Si HFET structure, grown by metal organic vapor phase epitaxy (MOVPE), is studied, with the details of the structure shown in Fig. 1. It consists of an AlN nucleation layer grown on a p-type conducting Si substrate, followed by a graded AlGaN layer to compensate the lattice mismatch between the substrate and the GaN, the carbon doped GaN layer (GaN:C), unintentionally doped GaN (uid GaN), and an AlGaN barrier on top. The 2DEG, forming the transistor channel, accumulates in the uid GaN layer just below the barrier. The graded AlGaN layer, starting as pure AlN at the substrate interface transforming to pure GaN at the GaN:C interface, was chosen to not introduce any hetero-interface between GaN:C and substrate that might lead to accumulation of free charges and/or hinder vertical charge flow. Aluminum concentration in the barrier, 2DEG density, and carbon concentration in the GaN:C of the wafer investigated are 25%, $\sim 6 \times 10^{12}\,\mathrm{cm}^{-2}$, and $\sim 5 \times 10^{18}\,\mathrm{cm}^{-3}$, respectively.

To characterize current flow in the device structure, a back biasing technique was employed. A voltage is applied to the conducting substrate. This affects the electrical fields in the layer structure. These fields impact the carrier concentration in the 2DEG (n_S), so monitoring n_S while applying a back bias reveals details about the electrical properties of layers between the substrate and the 2DEG. The setup used in this work is depicted in Fig. 1. More details on this technique can be found in Ref. 7.

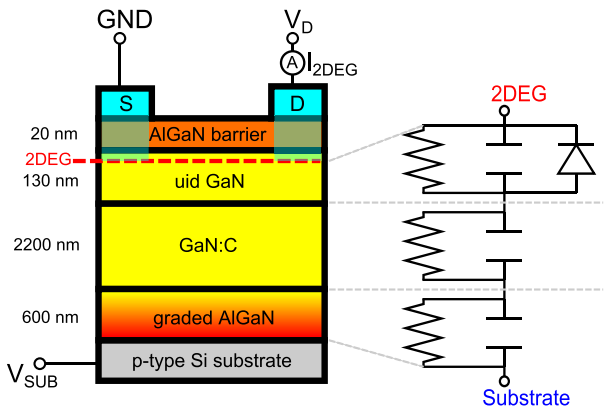

FIG. 1. Epitaxial AlGaN/GaN-on-Si structure investigated with contacts used for back bias characterization and equivalent circuit model.

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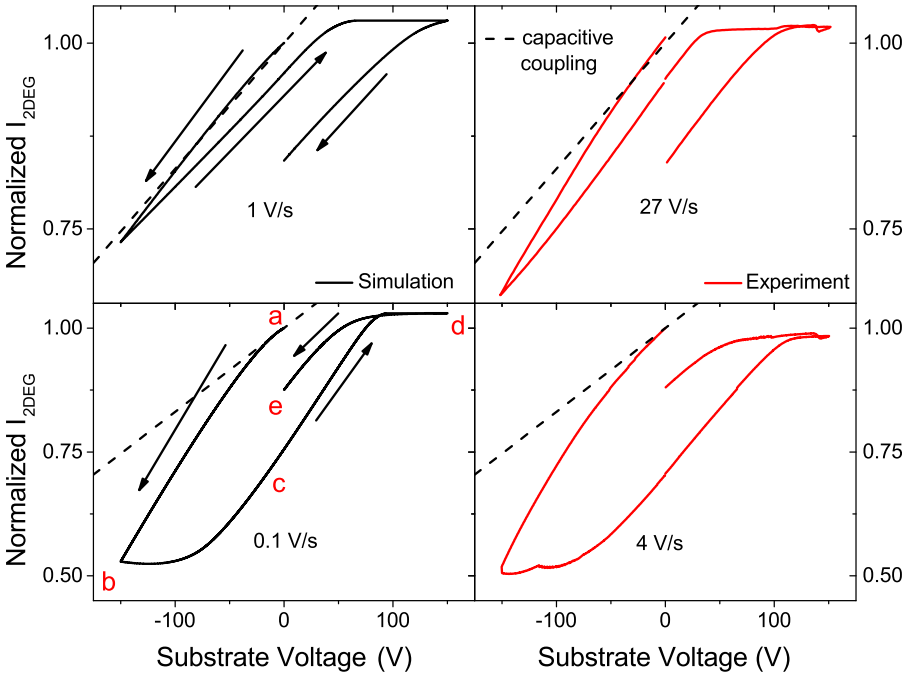

FIG. 2. Simulated (left) and measured (right) back bias sweeps are shown for fast (top) and slow (bottom) ramp rates. Arrows indicate the direction of the substrate voltage ramps. $V_D = 1$ V. The dashed line corresponds to the prediction of capacitive coupling.

An insulating buffer would lead to capacitive coupling between conducting substrate and 2DEG, resulting in a linear relation between V_{sub} and n_S. This behavior, associated with the capacitors of the equivalent circuit model also shown in Figure 1, is usually observed for small substrate voltages. If layers start to conduct and charging occurs, the ramped V_{sub} versus n_S relation begins to deviate from linear. Conducting layers are represented by resistors in the equivalent circuit model. In case of sudden changes in doping polarity at interfaces, pn junctions will also appear. In the structure tested in this work, such a rectifying junction is located at the uid GaN/GaN:C interface. All measurements have been made at room temperature.

III. SIMULATION DETAILS

Drift diffusion simulations were performed using Silvaco's Atlas Device Simulation Framework with activated Shockley-Read-Hall recombination and Fermi-Dirac statistics models. To represent n-type background doping in the uid GaN layer, $5 \times 10^{16}\,\mathrm{cm}^{-3}$ shallow donors are introduced. The carbon concentration in the GaN:C layer is set at $5 \times 10^{18}\,\mathrm{cm}^{-3}$ with the deep acceptor energy level at 0.9 eV above the valence band according to simulations in Ref. 13 under the assumption that carbon is incorporated mainly on nitrogen sites. Those deep acceptors are partially compensated by n-type background doping of $1.5 \times 10^{17}\,\mathrm{cm}^{-3}$. Doping in the graded AlGaN layer contains a shallow acceptor concentration of $1 \times 10^{18}\,\mathrm{cm}^{-3}$ representing the polarization induced charge in a linearly graded layer.[14] Those acceptors are fully compensated by shallow donors with a concentration of $1.5 \times 10^{18}\,\mathrm{cm}^{-3}$, which again are compensated by an acceptor with a concentration of $2 \times 10^{18}\,\mathrm{cm}^{-3}$ defined with constant energy below the conduction band, ensuring a smooth alignment of bands at the graded region's upper interface and a mid gap position at the interface with the Si substrate, causing insulating behavior. The nucleation layer is ignored in the simulation and the conducting Si substrate is represented as an electrode. No signs of deep depletion in the p-type Si, which would lead to an obvious reduction of overall vertical capacitance, were observed experimentally. The polarization charge at the AlGaN barrier/GaN interface is represented by a fixed charge of $0.017\,\mathrm{C/m}^2$. The polarization charge at the barrier surface is set to zero corresponding to full compensation by surface donors. Self heating and impact ionization are being neglected, since we are only concerned with the low field regime well below breakdown. The simulated temperature was 293 K for all simulations.

IV. RESULTS AND DISCUSSION

In Figure 2, results of a fast and a slow back bias ramp experiment are shown. The dashed lines in those graphs represent the expectations for capacitive coupling. In both graphs, the curve bends downwards at high negative back bias, corresponding to a reduction of current, exceeding what the capacitive coupling suggests. After sweeping back from negative back bias to 0 V, the current remains lower than it initially was, indicating a negative charge in the investigated layers. When ramping towards positive voltages afterward, the current continues to increase until a current level near the initial current is reached, where it saturates. On the ramp back to 0 V, the current again is reduced ending up at a current either further reduced or in between the former levels at 0 V substrate bias, depending on ramp rate. Vertical leakage currents are in the order of $\sim 1 \times 10^{-7}\,\mathrm{A/cm}^2$ throughout the measurements. Transient measurements, not shown here, reveal that the current reduction observed remains for several 100s of seconds, but is reversible by illumination with white light.

Ramp curves based on the simulations are also shown in Figure 2 and show excellent agreement. The ramp rates for agreement between simulation and experiment are

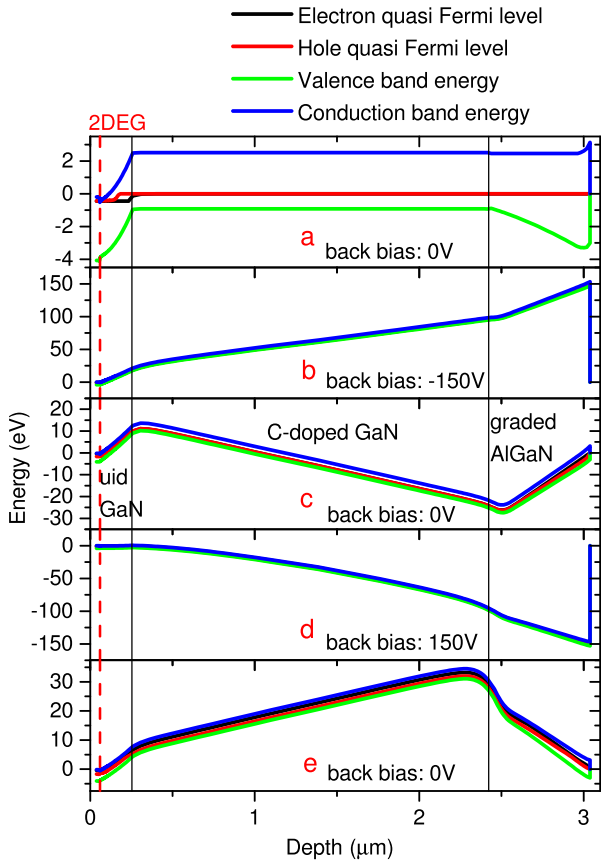

FIG. 3. Band diagrams during a back bias sweep, displayed against depth. Initially, the Fermi levels are leveled throughout, as no substrate bias has been applied yet (a). Under negative back bias (b), the bands are lifted on the substrate side. In the C-doped region, the bands are flattened. More voltage is, therefore, dropped across the uid GaN channel and the graded AlGaN layer. At 0 V substrate voltage after negative back bias (c), charge accumulation in the GaN:C results in a lift of the bands, whereas a lowering of the band energies is observed in the graded layer. Under positive back bias (d), the upper part of the structure is screened with most voltages dropped across the deeper layers. After negative and positive back bias (e), bands are lifted throughout, but mainly in the lower part of the GaN:C.

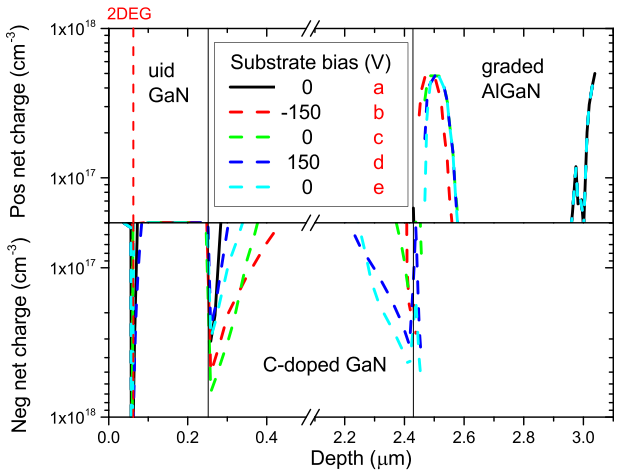

FIG. 4. Simulated net charge concentrations versus depth under bias conditions a to e, illustrating charge position and movement in the epitaxial structure on logarithmic scales for positive (upper half) and negative (lower half) net charges. Under negative back bias (b), a negative charge accumulates at the upper GaN:C interface, and a positive charge of similar size builds up in the graded layer. Both space charges remain after the back bias (c). Positive back bias (d) leads to an additional negative charge at the lower GaN:C interface, whilst the charge region at the upper interface is reduced in size.

surprisingly close given the essentially unknown compensation level with the remaining difference in ramp rate reflecting a difference in the thermally activated hole density in the GaN. To explain the charging effects, we will focus on the slower ramp rate simulation. The good agreement between experiment and simulation suggests that the assumed carbon level of 0.9 eV above the valence band is correct, since simulation results are very sensitive to changes of the dominant dopant's energy level. Also the good agreement suggests that the observations can be explained by effects based only on the physics simulated by the software. Hence, vertical leakage through the uid GaN layer as observed for both samples in Ref. 7, other trap assisted tunneling effects related to high electric fields, or radiative recombination caused by hot electrons as described in Ref. 15 do not significantly influence the observed behavior. The measured vertical leakage is higher than the simulated displacement currents, which are less than 1×10^{-8} A/cm^2. We assume that the measured leakage is caused by local leakage paths appearing along some extended defects mainly under the ohmic contacts similar to the findings in Ref. 16. We still get the good agreement between experiment and simulation, because these leakage paths are highly localized, whereas the substrate ramp measurement is sensitive to the field averaged over the entire source/drain gap area.

For the sample investigated here, Figures 3 and 4 show simulated band diagrams and charge position during the back bias ramp. Figure 3(b) shows that flattening of bands in the GaN:C region and increasing the electrical fields in the adjacent layers cause the extended current reduction under negative back bias. The reason for the flattening can be deduced from Figure 4, where the formation of positive and negative space charges under negative back bias is depicted. Near the 2DEG carbon, acceptor states are ionized, creating free holes that move towards the substrate where they are trapped, partially neutralizing deep acceptors in the graded layer and creating the positive space charge. After the back bias (c), the space charges remain, causing the current reduction shown in Figure 2 after moderate −150 V bias.

As shown in Figure 2, ramping to a positive back bias of 150 V subsequently results in I_{2DEG} saturation near the initial current level. This is due to the injection of electrons into the structure via the forward biased np junction between 2DEG and GaN:C (Figure 3(d)). The injected electrons are trapped by acceptor states in the GaN:C, mainly at the GaN:C/graded AlGaN interface. The resulting negative charge screens the 2DEG from the substrate bias and keeps the electric field below the channel constant. In case of the slow ramp, the number of thermally generated holes in the GaN:C region, which are created during the positive ramp, is sufficient to mostly neutralize the excess ionized acceptor charge at the top interface. The result is described by Figures 3(e) and 4. Though the injected electrons create a significant negative charge at the bottom of the GaN:C, the ionized acceptor concentration at the top is reduced. The impact of charge on n_S is weighted by its distance to the 2DEG based on classical electrostatics: $q\Delta n_S = -\int yQ(y)dy$. As the charges at the top

interface are much closer to the 2DEG, their effect on n_S is far greater, explaining less reduction of I_{2DEG} after the positive back bias ramp. It is important to notice that the simulation does not suggest any electron injection from the substrate into the epitaxial structure. The charge redistribution within the GaN:C layer on its own is obviously sufficient to explain the observed behavior. Experimentally, electron injection from the Si substrate is likely to occur associated with vertical leakage;[17] however, any electron trapping would most likely be localized to those leakage paths and hence would not strongly impact our measurements. The fact that the experimentally observed current reduction lasts for a period of several 100s of seconds and that recovery can be accelerated by white light illumination is perfectly explained by the ionized deep acceptor states being its main cause.

The current collapse after negative back bias implies high dynamic on-resistance and serious current instabilities under field polarities corresponding to those of a device with grounded substrate and positive voltage applied to the drain contact, making the device unsuitable for power applications. The investigated sample obviously lacks a vertical leakage path for holes from the 2DEG.[7] Intentional incorporation of dislocations into the uid GaN, which presumably establishes the vertical leakage path, could prevent the current collapse, but increasing the defect density is also likely to come with other detrimental effects. The ionization and redistribution of charges in the carbon doped GaN discussed here also impact its beneficial effect regarding vertical breakdown, as the described effects cause increased voltage drop and therefore higher electrical fields in the adjacent layers. Keeping the thickness of such a layer reasonably thin in relation to the overall epitaxial structure is therefore desirable.

V. CONCLUSION

A reduction of 2DEG current after back bias application of both polarities has been shown for a GaN HFET structure containing a carbon doped layer. Thermally activated hole flow, trapping within the GaN:C layer and electron injection into the layer structure from the 2DEG have been identified as the origin with the help of simulations. As the current reduction is linked to acceptor trap states with long lifetimes, it will cause strong current collapse.

This paper clearly shows and explains that detrimental effects for GaN-based power devices linked to the carbon doped layer can occur. It is essential to take these effects into account to keep the benefits of carbon doping whilst providing reliable AlGaN/GaN/GaN:C based devices.

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